

**Claims:**

1. A low-impact universal interface for analyzing a SCSI bus with a digital logic analyzer comprising:

5 a SCSI bus interface connector that connects said universal interface to said SCSI bus;

one or more transceivers connected to said SCSI bus interface connector that convert a set of low voltage differential input signals to a set of single ended transceiver output signals;

10 a field programmable gate array controller that receives said set of single ended transceiver output signals and provides programmed post-processing to at least a portion of said set of single ended transceiver output signals;

a programmable clock connected to said field programmable gate array controller that produces a programmed clock signal that is utilized by said digital logic analyzer to  
15 synchronize data sampling on said SCSI bus;

an erasable programmable read-only memory circuit connected to said field programmable gate array controller that provides programming information for said post-processing;

20 a set of field programmable gate array controller output signals produced by said field programmable gate array controller; said set of field programmable gate array controller output signals that include an output clock signal and one or more trigger signals; and,

an analyzer output connector that receives said set of single ended transceiver output signals and said set of field programmable gate array controller output signals and produces a digital logic analyzer input.

2. A device of claim 1 wherein said field programmable gate array controller determines the direction of transfer between said analyzer and a target on said SCSI bus and acts as a free running clock that transmits said output clock signal to said analyzer.

3. A device of claim 2 wherein said output clock signal is said programmed clock signal when no data transfer is in progress, said output clock signal is phase locked to request

during a data-in transfer, and said output clock signal is phase locked to acknowledge during data-out transfer.

4       A device of claim 1 wherein said field programmable gate array controller is re-programmed to accept and execute new testing protocols.

5.       A device of claim 1 wherein said universal interface further comprises a programming link to said field programmable gate array controller to download programming to said field programmable gate array controller from an external computer source.

6.       A device of claim 1 wherein said universal interface further comprises an external trigger controller connected to said field programmable gate array controller to introduce external trigger commands said universal interface.

7.       A device of claim 1 wherein said universal interface is impedance matched to said SCSI bus to minimize noise introduced by said universal interface.

8.       A device of claim 1 wherein said transceivers are configured with a receive interface to said SCSI bus, and a transmit interface to said digital logic analyzer.

9.       A device of claim 1 wherein said transceivers are low capacitance with a load matching to that of a computer hard drive.

10.      A method of interfacing a SCSI bus with a digital logic analyzer with an analyzer interface board to analyze a SCSI bus protocol comprising:

          connecting to said SCSI bus with a SCSI bus interface connector on said analyzer interface board;

5           applying power to said analyzer interface board;

transferring data on said SCSI bus to one or more transceivers on said analyzer interface board that convert a set of low voltage differential signals to a set of single ended transceiver output signals;

receiving and post-processing at least a portion of said set of single ended transceiver  
10 output signals with said field programmable gate array controller;

applying a programmable clock signal to said field programmable gate array controller with a programmable clock to provide an output clock signal that is utilized by said digital logic analyzer to synchronize data sampling on said SCSI bus;

providing programming information for said post-processing with an erasable  
15 programmable read-only memory circuit connected to said field programmable gate array;

producing a set of field programmable gate array controller output signals with said field programmable gate array controller that include said output clock signal and one or more trigger signals; and,

receiving said set of single ended transceiver output signals and said set of field  
20 programmable gate array controller output signals to produce a digital logic analyzer input at an analyzer output connector.

11. A method of claim 1 wherein said step of receiving and post-processing at least a portion of said set of single ended transceiver output signals with said field programmable gate array controller further comprises:

determining the direction of transfer between said analyzer and a target on said SCSI  
5 bus; and,

transmitting said output clock signal to said analyzer with said field programmable gate array controller that is based upon said direction of transfer.

12. A method of claim 1 wherein said step of receiving and post-processing at least a portion of said set of single ended transceiver output signals with said field programmable gate array controller further comprises:

determining the direction of transfer between said analyzer and a target on said SCSI  
5 bus;

transmitting said output clock signal to said analyzer with said field programmable gate array controller as said programmed clock signal when no data transfer is in progress;

transmitting said output clock signal to said analyzer with said field programmable gate array controller as a phase locked to request during a data-in transfer; and,

10 transmitting said output clock signal to said analyzer with said field programmable gate array controller as said output clock signal is phase locked to acknowledge during data-out transfer.

13. A method of claim 1 further comprising the step of:

re-programming said field programmable gate array controller to accept and execute additional test protocols.

14. A method of claim 1 further comprising the step of:

downloading programming to said field programmable gate array controller with a programming link from an external computer source.

15. A method of claim 1 further comprising the step of:

introducing an external trigger command to said universal interface with an external trigger controller connected to said field programmable gate array.

16. A method of claim 1 further comprising the step of:

minimizing noise introduced by said universal interface by impedance matching said universal interface to said SCSI bus.

17. A method of claim 1 wherein said step of receiving and post-processing at least a portion of said set of single ended transceiver output signals with said field programmable gate array controller further comprises:

5 configuring said transceivers with a receive interface to said SCSI bus, and a transmit interface to said digital logic analyzer.

18. A method of claim 1 further comprising the step of:

load matching capacitance of said transceivers to that of a computer hard drive.

19. A low-impact universal interface means for analyzing a SCSI bus with a digital logic analyzer comprising:

a SCSI bus interface connector means for connecting said universal interface to said SCSI bus;

5 one or more transceiver means connected to said SCSI bus interface connector for converting a set of low voltage differential input signals to a set of single ended transceiver output signals;

a field programmable gate array controller means for receiving said set of single ended transceiver output signals and providing programmed post-processing to at least a  
10 portion of said set of single ended transceiver output signals;

a programmable clock means connected to said field programmable gate array controller means for providing a programmed clock signal that is utilized by said digital logic analyzer to synchronize data sampling on said SCSI bus;

an erasable programmable read-only memory circuit means connected to said field  
15 programmable gate array controller means for providing programming information for said post-processing;

a set of field programmable gate array controller output signal means produced by said field programmable gate array controller means; said set of field programmable gate array controller output signal means that include an output clock signal and one or more  
20 trigger signals; and,

an analyzer output connector means for receiving receives said set of single ended transceiver output signals and said set of field programmable gate array controller output signal means for producing a digital logic analyzer input.